CLAIMS

Please **CANCEL** claims 23-26 as follows:

A status of the claims is provided below.

Claim 1. (original) A method of manufacturing a semiconductor structure, comprising the steps of:

forming a p-type field-effect-transistor (pFET) channel and a n-type field-effect-transistor (nFET) channel in a substrate;

providing a first layer of material within the pFET channel having a lattice constant different than the lattice constant of the substrate;

providing a second layer of material within the nFET channel having a lattice constant different than the lattice constant of the substrate;

forming an epitaxial semiconductor layer over the first layer of material in the pFET channel and the second layer of material in the nFET channel, the epitaxial semiconductor layer having substantially a same lattice constant as the substrate such that a stress component is created within the pFET channel and the nFET channel.

Claim 2. (original) The method of claim 1, wherein the pFET channel and the nFET channel are formed simultaneously.

Claim 3. (original) The method of claim 1, wherein the pFET channel and the nFET channel are formed separately.

Claim 4. (original) The method of claim 1, wherein the first layer of material is SiGe having a content of Ge approximately greater than 25% in ratio to Si.

Claim 5. (original) The method of claim 4, wherein the first layer of material creates a tensile stress within the epitaxial semiconductor layer of greater than 3 GPa.

Claim 6. (original) The method of claim 1, wherein the second layer of material is SiGe.

Claim 7. (original) The method of claim 6, wherein the second layer of material creates a tensile stress within the epitaxial semiconductor layer within the nFET channel.

Claim 8. (original) The method of claim 1, wherein the first layer of material is Si:C.

Claim 9. (original) The method of claim 1, further comprising the steps of:

forming a gate oxide structure over the epitaxial semiconductor layer; and

forming extensions and a drain region and a source region in the substrate on sides of the gate oxide structure.

Claim 10. (original) The method of claim 1, wherein the forming of the nFET and pFET channel includes etching the Si layer to approximately a depth of about 200Å to 400Å.

Claim 11. (original) The method of claim 1, wherein:

the first layer of material is formed by placing a hard mask over the nFET channel and growing the first layer of material within the pFET channel; and

the second layer of material is formed by placing a hard mask over the pFET channel and growing the second layer of material within the nFET channel.

Claim 12. (original) The method of claim 1, further comprising forming shallow trench structures within the substrate.

Claim 13. (original) The method of claim 1, wherein the first layer of material and the second layer of material are grown to a height about 100 Å to 300 Å.

Claim 14. (original) The method of claim 1, wherein the substrate layer is silicon on insulator.

Claim 15. (original) The method of claim 1, wherein the first layer of material and the second layer of material are both SiGe material, having a larger Ge percentage than approximately 25% to 30% to apply for the pFET.

Claim 16. (original) A method of manufacturing a semiconductor structure, comprising the steps of:

forming a p-type field-effect-transistor (pFET) channel and a n-type field-effect-transistor (nFET) channel in a substrate;

providing a first layer of material within the pFET channel having a lattice constant different than the lattice constant of the substrate;

providing a second layer of material within the nFET channel having a lattice constant different than the than the lattice constant of the substrate; and

forming an epitaxial semiconductor layer over the first layer of material in the pFET channel and the second layer of material in the nFET channel, the epitaxial semiconductor layer having substantially a same lattice constant as the substrate thus creating a stress component opposite to that of the first layer of material within the pFET channel and the second layer of material within the nFET channel.

Claim 17. (original) The method of claim 16, wherein the pFET channel and the nFET channel are formed simultaneously.

Claim 18. (original) The method of claim 16, wherein the pFET channel and the nFET channel are formed separately.

Claim 19. (original) The method of claim 16, wherein the first layer of material is Si:C and the second layer of material is SiGe.

Claim 20. (original) The method of claim 19, wherein:

the first layer of material creates a compressive stress within the epitaxial semiconductor layer within the pFET channel;

and the second layer of material creates a tensile stress within the epitaxial semiconductor layer within the nFET channel.

Claim 21. (original) The method of claim 16, further comprising the steps of:

forming a gate oxide structure over the epitaxial semiconductor layer; and

forming extensions and a drain region and a source region in the Si layer on sides of the gate oxide structure.

Claim 22. (original) The method of claim 16, wherein:

the first layer of material is formed by placing a hard mask over the nFET channel and growing the first layer of material within the pFET channel; and

the second layer of material is formed by placing a hard mask over the pFET channel and growing the second layer of material within the nFET channel.

Claims 23-26. (canceled)